# GALILEO

Changing the world of FPGA design.

Galileo Logic Explorer (tm)

Galileo Logic Explorer combines leading edge VHDL or Verilog synthesis support with architecture-specific optimization for all popular device types. Module Generation libraries maximize design reuse by providing technology-specific implementations of complex functions and operators.

Synthesis And Its Role In The Overall Design Cycle
Galileo is more than just logic synthesis. Exemplar's Galileo tool suite works with your existing place and route tools to accomplish the entire design cycle from design entry to timing verification.
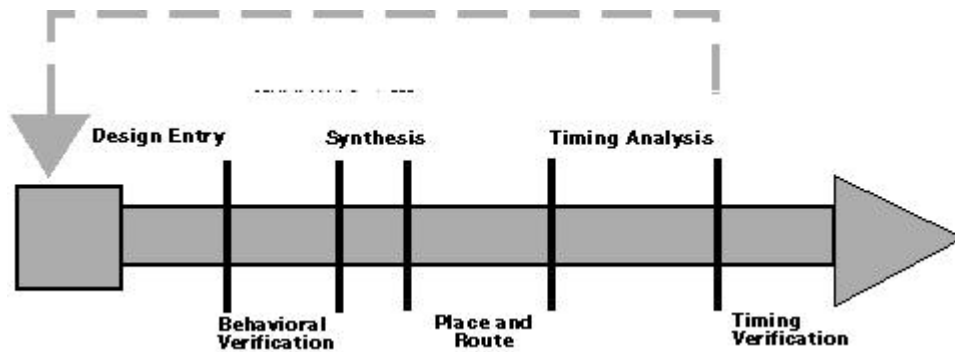
Synthesis plays an important role in your design cycle. Accurate, efficient synthesis results are key to reducing the number of design iterations. Control over the synthesis process is key. By allowing you to identify the critical paths in your circuit without

creating full simulation test benches, Galileo enables you to focus your attention on the critical aspects of your design.

Synthesis
The increasing complexity of FPGA, CPLD and ASIC design requires the use of Hardware Description Languages (HDLs) for design entry. Exemplar Logic supports both the VHSIC Hardware Description Language (VHDL) and the Verilog HDL at the Register Transfer Level (RTL), dataflow level, and at the netlist level. Support of HDL constructs is at the leading-edge in the industry and assures design entry at the highest level of abstraction.

Module Generation
High-level design allows the use of operators such as adders, multipliers, comparators, incrementors, shifters, and muxes indiscriminately. Without an understanding of the target technology however, the final implementation may be highly inefficient. Galileo's Module Generation is packed with technology-specific implementations of high-level functions and operators. Module Generators are highly optimized for different architectures and include are and delay trade-offs, while supporting data paths of varying sizes.

Architecture Specific Optimization
At the center of Galileo Logic Explorer resides a set of embedded optimization techniques developed for each supported technology, with detailed knowledge about how logic is implemented to take maximum advantage of unique device architectures. It improves a circuit design by optimizing it for the target technology within a given set of performance and area constraints. Device-specific optimization ensures that your designs can be implemented on smaller, less expensive devices to meet performance specifications.

Exemplar Logic pioneered the concept of using technology-specific algorithms for FPGA and CPLD design, such as fanin-limited, cube-based and mux-based optimization. It was the first to introduce FPGA-specific technology mapping: Look-Up Table (LUT) mapping for LCA-based architectures, clock enable detection, complex i/o support and product term expanders utilization, for example.

Applications
- High-level design for FPGAs, and CPLDs
- FPGA and CPLD retargeting to ASICs
- ASIC prototyping
- PAL and PLD design migration to FPGAs

Key Features Of Logic Explorer
- Full support for synthesizable Verilog HDL and VHDL
- Comprehensive error checking and reporting
- Meets HDL standards, IEEE 1076-1993 and 1164, VHDL standards, OVI 2.0
- standards, and Verilog-XL compliant.
- Technology-specific optimization algorithms exploit device features for better
- area/speed performance
- Module Generation for structured logic synthesis and design re-use.
- User control over are and delay constraints.

Input And Output Formats
VHDL, Verilog HDL , EDIF, and XNF

Galileo Time Explorer(tm)

Galileo Time Explorer is a powerful design analysis tool for synthesized as well as non-synthesized designs. Time Explorer can be used within the Galileo design environment, with Galileo Logic Explorer and Galileo V-System simulator, or with other simulators.

Time Explorer: Three Modules For Timing Verification
TimeScope performs static timing analysis with concise critical path and point-to-point delay reporting. NetScope generates schematics, including critical path highlights through cross-probing with the static timing analyzer. TimeShuttle translates and back-annotates post place and route netlists for VHDL and Verilog gate-level timing simulation using SDF and standards.

TimeScope Static Timing Analysis
TimeScope provides a comprehensive timing analysis utility that handles pre-place and route (estimated) as well as post-place and route (accurate) timing information. Static timing analysis is important in verifying timing performance and correctness of a circuit. Timing analysis traces clocks to sequential gates, computes delay among various paths in the circuit and identifies critical paths, without the need for generating and applying stimulus vectors for the circuit.

NetScope Schematic Generator/Viewer
Netlists can be graphically represented with NetScope, a schematic generator and viewer provided with Time Explorer. NetScope allows zoom-in, zoom-out and object search, multiple page schematics, postscript printing, and EDIF schematic out facilities. Popular FPGA symbol libraries are provided and other symbol libraries may be obtained from third-party vendors.

TimeShuttle Simulation Interface
Gate-level simulation is the final verification step before committing to a device. TimeShuttle provides an interface between device-specific, timing annotated netlists and standard VHDL or Verilog HDL simulators. This allows the designer to use the same simulator at the specification phase and at the gate-level verification phase of the design, and eliminates the cumbersome process of re-entering test vectors. Simulation libraries are provided, and are based on VITAL and SDF standards.

Key Features Of Time Explorer
- Critical path analysis and comprehensive report generation
- Point-to-point static timing analysis and highlighting to a schematic
- Pre- and post-place and route schematic generation, viewing, and plotting.
- VITAL compliant simulation libraries
- SDF read/write back-annotation facility

TimeScope Static Timing Analysis
- Pre-place and route for all technologies
- Post-place and route for SDF and back-annotated XNF

TimeShuttle Simulation Interfaces
 Pre/post-place and route VITAL libraries for

- Xilnix LCA
- Actel ACT
- Altera MAX and FLEX
- Lucent Technologies ORCA

Galileo V-System Simulator

Galileo V-System simulator is used to simulate VHDL designs from the behavioral level through post-layout at the gate level and is fully integrated with the Galileo Logic Explorer and Time Explorer design modules.

VHDL Simulation
Galileo V-System is a complete VHLD compiler and simulator system, with support for IEEE Std. 1076-(1987 and -1993) and 1164. The state-of-the-art compiler and simulator technology used in Galileo V-System was developed by Model Technology Incorporated, the VHDL simulator market leader.

VITAL Acceleration
V-System if fully VITAL level 1 compliant with built-in acceleration of VITAL primitives at the gate level and SDF back-annotation support.

Powerful Debug Environment
Use the best VHDL debugging environment available today: dynamically-linked windows show design hierarchy, VHDL source code, VHDL processes, current values of signals, generics and variables.

Waveform Display
View any signal of any type -- in hex, octal or binary -- from anywhere in the design. Display signals of all types, including user-defined.

Fast Direct Compile Technology
The best of both worlds: compilation times as fast as any interpreted simulator, simulation times faster than C-compiled tools. Compiled models are "object compatible" across all platforms.

External Interfaces
Galileo V-System for the workstation features interfaces with the SmartModel library, foreign languages (allowing the use of C language models) and TSSI vector format.

Highlights

- Full Compliance VHDL Compiler & Simulator
- Supports both IEEE Std. 1076-(1987 & -1993) and 1164 in same design
- VITAL gate level acceleration & SDF support
- Fast direct compile technology
- Includes source language debugger, waveform display and design browser
- PC Windows, SunSPARCstation, HP 700 support